

WHAT IS CLAIMED IS:

1           1.     A method of transmission between two processors arranged inside a radio  
2 communication unit and linked together by a connection internal to the radio communication  
3 unit, the first processor executing at least one application and the second processor executing  
4 radio communication operations between said unit and outside communication units, comprising:  
5                 apportioning of codes by one of the two processors, the sender of said codes, into  
6 frames having respective lengths;  
7                 writing of elements by the sending processor into dedicated fields of each frame,  
8 the elements comprising:  
9                     the length of the frame,  
10                    a value of an indicator of transmission error determined by the sending  
11 processor on the basis of certain at least of the codes placed in the frame, and  
12                    a start of frame indicator and an end of frame indicator;  
13                 transmitting of the frames by the internal connection;  
14                 for each frame, verifying by the other processor, the receiver of said codes:  
15                     the identity between the length of the frame received and the length  
16 written,  
17                     the identity between the written value of the error indicator and a value of  
18 this error indicator as determined by the receiving processor on the basis of certain at least of the  
19 codes received in the frame, and  
20                 the presence of the start and end of frame indicators;

21                   in the case of positive verifications, producing by the receiving processor of an  
22 acknowledgement message dispatched to the sending processor by the internal connection.

1           2.     The method according to Claim 1, further comprising by the receiving processor  
2 verifying that the start indicator of a second frame received just after a first frame, according to  
3 the chronological order of reception of the frames, is received after a specified separation time  
4 interval from the reception of the end indicator of said first frame.

1           3.     The method according to Claim 1, wherein the frames comprise at least one  
2 control field containing a code for distinguishing between several types of frames.

1           4.     The method according to Claim 1, further comprising:  
2                   sending a frame via the internal connection in response to a primitive of a first  
3 type produced within the sending processor; and  
4                   producing a primitive of a second type within the receiving processor in response  
5 to the reception of the frame by the internal connection.

1           5.     The method according to Claim 1, wherein the frame contains codes for  
2 requesting end of transmission by the internal connection, and is sent prior to an interruption of  
3 operation of the sending processor.

1           6.     The method according to Claim 5, wherein the codes for requesting end of  
2     transmission comprise codes indicating the state of the sending processor after the interruption of  
3     operation of the sending processor.

1           7.     The method according to Claim 1, wherein the value of the transmission error  
2     indicator is given by the remainder after dividing a polynomial constructed on the basis of  
3     certain at least of the codes contained in the frame by a generating polynomial.

1           8.     The method according to Claim 1, wherein the codes correspond to information  
2     contained in packets, and wherein the sending processor apportions the codes corresponding to  
3     the information of a packet into a single frame associated with said packet.

1           9.     The method according to Claim 8, wherein said packet is a data packet or a  
2     signaling packet.

1           10.    The method according to Claim 3, wherein the codes correspond to information  
2     contained in packets, the sending processor apportioning the codes corresponding to the  
3     information of a packet into a single frame associated with said packet, each packet being of a  
4     predefined type, and wherein the type of the frame associated with a packet is determined as a  
5     function of the type of the packet.

1           11.    The method according to Claim 10, wherein

2                   an I frame of the HDLC protocol is associated with a packet of data intended for  
3 or emanating from the application or a control packet,  
4                   a UI frame of the HDLC protocol is associated with a packet transporting voice,  
5 and  
6                   a U SABM, UA, DISC or DM frame is associated with the signaling of the  
7 communication.

1           12.    The method according to Claim 1, wherein an S frame of the HDLC protocol is  
2 used to send a message for supervising a transmission by the internal connection.

1           13.    A processor including an interface for connecting another processor, comprising:  
2                    means for producing frames containing codes apportioned into specified fields;  
3                    means for determining the value of a transmission error indicator on the basis of  
4   certain at least of the codes placed in a frame;  
5                    means for writing elements into dedicated fields of each frame, the elements  
6   including:  
7                    a length of the frame,  
8                    a specified value of the error indicator determined for the frame, and  
9                    a start of frame indicator and an end of frame indicator;  
10                  means for sending frames via said interface;  
11                  means for receiving frames via said interface;  
12                  means for measuring the length of a frame received;  
13                  means for verifying in a frame received:  
14                    an identity between the length measured of the frame received and the  
15   length written,  
16                    an identity between the written value of the error indicator in the frame  
17   received and a value of this error indicator as determined on the basis of certain at least of the  
18   codes received in the frame, and  
19                    a presence of the start and end of frame indicators;

20 means for producing acknowledgement messages devised so as to dispatch an  
21 acknowledgement message via said interface in response to a frame received validated by the  
22 verification means.

1 14. The processor according to Claim 13, further comprising means for measuring a  
2 duration between the reception of the start indicator of a second frame received via said interface  
3 after a first frame, according to the chronological order of reception of the frames, and the  
4 reception of the end indicator of said first frame and, comprising means for verifying that said  
5 duration is greater than a specified separation time interval.

1 15. The processor according to Claim 13, further comprising means for writing a type  
2 of frame code into at least one control field of each frame.

1 16. The processor according to Claim 13, further comprising means for producing  
2 primitives, wherein the means for sending the frames via said interface are devised in such a way  
3 as to send a frame containing determined codes in response to a primitive of a first type produced  
4 within said processor, and wherein the means for producing primitives are devised so as to  
5 produce a primitive of a second type in response to a frame containing determined codes  
6 received by said interface.

1 17. The processor according to Claim 13, wherein the means for sending the frames  
2 are devised so as to send via said interface a frame containing codes for requesting end of  
3 transmission prior to an interruption of operation of the processor.

1           18.    The processor according to Claim 17, wherein the means for sending the frames  
2   comprise means for introducing into the frame containing the codes for requesting end of  
3   transmission, codes indicating the state of the processor after the interruption of operation of the  
4   processor.

1           19.    The processor according to Claim 13, wherein the means for determining the  
2   value of the error indicator comprise means for calculating the remainder of dividing a  
3   polynomial constructed on the basis of certain at least of the codes contained in a frame by a  
4   generating polynomial.

1           20.    The processor according to Claim 13, wherein the codes correspond to  
2   information contained in packets, and wherein the means for apportioning the codes are devised  
3   so as to apportion the codes corresponding to the information of a packet into a single frame  
4   associated with said packet.

1           21.    The processor according to Claim 15, wherein the codes correspond to  
2   information contained in packets, the means for apportioning the codes being devised so as to  
3   apportion the codes corresponding to the information of a packet into a single frame associated  
4   with said packet, each packet being of a predefined type, and wherein the means for producing  
5   the frames are devised so as to associate with a packet a frame of specified type determined as a  
6   function of the type of the packet.

1           22.     The processor according to Claim 21, wherein the means for producing the frames  
2     are devised so as to associate an I frame of the HDLC protocol with a data packet, and so as to  
3     associate a U frame of the HDLC protocol with a signalling packet.

1           23.     The processor according to Claim 13, wherein the means for producing the frames  
2     are devised so as to produce an S frame of the HDLC protocol to send a message for supervising  
3     a transmission via said interface.

1           24.     The processor according to Claim 13, comprising means for executing an  
2     application, means for processing, according to said application, information corresponding to a  
3     part of the codes contained in frames received via said interface, and means for producing codes  
4     to be apportioned into frames using the information produced by said application.

1           25.     The processor according to Claim 13, comprising means for executing operations  
2     of radio communication with outside communication units, means for producing radio signals  
3     transmitted using a part of the codes contained in frames received via said interface, and means  
4     for producing codes to be apportioned into frames using the radio signals received.



1           26.    A radio communication unit, comprising:  
2                   a first processor;  
3                   a second processor;  
4                   an internal interface interconnecting the first and second processors;  
5                   the first processor including:  
6                         means for executing an application; and  
7                         a communications protocol to transmit frames over, and receive frames  
8 from, the internal interface;  
9                   the second processor including:  
10                        means for executing operations of external radio communication; and  
11                        the communications protocol to transmit frames over, and receive frames  
12 from, the internal interface;  
13                   wherein the communications protocol at the first and second processor provides a  
14 security function by encapsulating processor packet data in the frame with at least one security  
15 field and decapsulating the frame to confirm correct receipt of the packet data by verifying  
16 security data in the at least one security field.

1           27.    The radio communication unit according to Claim 26, wherein the  
2 communications protocol at the first and second processor further transmits an acknowledgment  
3 message in response to a received and confirmed frame.

1        28.    The radio communication unit according to Claim 26, wherein the  
2    communications protocol at the first and second processor determines data for inclusion in the  
3    security field based at least in part on the processor packet data.

1           29.    A method for inter-processor communication wherein a first and second processor  
2   are located within a communication unit and are interconnected by an internal interface,  
3   comprising:

4                   encapsulating a communications packet originated by the first processor in a  
5   secure frame which includes a data field containing the communications packet and at least one  
6   security field containing security data derived at least in part from the encapsulated  
7   communications packet;

8                   transmitting the secure frame over the internal interface to the second processor;

9                   decapsulating the secure frame by the second processor to recover the at least one  
10   security field containing security data and the data field containing the communications packet;

11                  verifying the security data to confirm correct receipt of the communications  
12   packet; and

13                  sending of an acknowledgment from the second processor to the first processor  
14   over the internal interface in response to the verification.

1           30.    The method according to Claim 29, wherein the at least one security field  
2   comprises a length field containing data indicative of a length of the secure frame which  
3   encapsulates the communications packet, and wherein verifying comprises checking that a length  
4   of the received secure frame matches the length in the length field.

1           31.    The method according to Claim 29, wherein the at least one security field  
2    comprises an error detection field containing redundancy check data for the secure frame which  
3    encapsulates the communications packet, and wherein verifying comprises checking that  
4    redundancy check data calculated for the received secure frame matches the redundancy check  
5    data contained in the error detection field.

1           32.    The method according to Claim 29, wherein encapsulating further comprises  
2    providing the secure frame with a start of frame and an end of frame indicator, and further  
3    comprising:  
4                decapsulating the secure frame by the second processor to recover the start of  
5    frame and end of frame indicators;  
6                verifying that the start of frame and end of frame indicators are present; and  
7                sending of the acknowledgment from the second processor to the first processor  
8    over the internal interface in response to the verification.

1           33.    The method according to Claim 29, wherein the second processor receives  
2    consecutive first and second secure frames, and further comprising:  
3                measuring a time interval between the first and second secure frames;  
4                verifying that the time interval exceeds a threshold; and  
5                sending of the acknowledgment of the second secure frame from the second  
6    processor to the first processor over the internal interface in response to the verification.

1           34.    A communication unit, comprising:

2                   a first and second processor located within the communication unit;

3                   an internal interface interconnecting the first and second processors;

4                   wherein the first processor includes a communications protocol to:

5                               encapsulate a communications packet in a secure frame which includes a  
6   data field containing the communications packet and at least one security field containing  
7   security data derived at least in part from the encapsulated communications packet; and

8                               transmit the secure frame over the internal interface to the second  
9   processor; and

10                  wherein the second processor includes a communications protocol to:

11                              decapsulate the secure frame to recover the at least one security field  
12   containing security data and the data field containing the communications packet;

13                              verify the security data to confirm correct receipt of the communications  
14   packet; and

15                              send an acknowledgment to the first processor over the internal interface  
16   in response to the verification.

1           35.    The unit according to Claim 34, wherein the at least one security field comprises a

2   length field containing data indicative of a length of the secure frame which encapsulates the

3   communications packet, and wherein the second processor communications protocol verification

4   checks that a length of the received secure frame matches the length in the length field.

1           36.    The unit according to Claim 34, wherein the at least one security field comprises  
2   an error detection field containing redundancy check data for the secure frame which  
3   encapsulates the communications packet, and wherein the second processor communications  
4   protocol verification checks that redundancy check data calculated for the received secure frame  
5   matches the redundancy check data contained in the error detection field.

1           37.    The unit according to Claim 34, wherein the first processor communications  
2   protocol encapsulation further provides the secure frame with a start of frame and an end of  
3   frame indicator, and wherein the second processor communications protocol:  
4                decapsulates the secure frame to recover the start of frame and end of frame  
5   indicators;  
6                verifies that the start of frame and end of frame indicators are present; and  
7                sends the acknowledgment to the first processor over the internal interface in  
8   response to the verification.

1           38.    The unit according to Claim 34, wherein the second processor receives  
2   consecutive first and second secure frames, and the second processor communications protocol  
3   further:  
4                measures a time interval between the first and second secure frames;  
5                verifies that the time interval exceeds a threshold; and

6                    sends the acknowledgment of the second secure frame to the first processor over  
7 the internal interface in response to the verification.

1            39.    The unit according to Claim 34, wherein the communications protocol used by the  
2 first and second processors comprises a transport level protocol.

1            40.    The unit according to Claim 39, wherein the transport level protocol is host  
2 controller interface secure transport layer protocol.